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15. (Amended) A semiconductor device having at least two levels of interconnecting metallurgy, said semiconductor device comprising:

a first level of substantially silicide free metallurgy; and

an uppermost layer of metallurgy including a bonding pad, wherein a top of said uppermost layer comprises a silicided surface,

wherein an increase in thickness of said uppermost layer with respect to the thickness of said first level of substantially free metallurgy reduces sensitivity to resistivity shifts associated with said silicided surface.

21. (Amended) A semiconductor device comprising:

an exterior surface having a top level of metallurgy,

wherein an exposed portion of said top level of metallurgy comprises a bonding pad,

wherein an upper 10% to 20% of said bonding pad comprises a silicided surface, and

wherein an increase in thickness of said top level of metallurgy with respect to thicknesses of other metallurgy layers within said device reduces sensitivity to resistivity shifts associated with said silicided surface.

Please cancel claim 27 without prejudice or disclaimer

29. (Amended) A semiconductor chip comprising:

an exterior surface having a top level of metallurgy; and

an interior having at least one internal level of metallurgy,

wherein said top level of metallurgy has an increased thickness than said internal level of metallurgy,

wherein an exposed portion of said top level of metallurgy comprises a bonding pad,

wherein an upper 10% to 20% of said bonding pad comprises a silicided surface, and

wherein said increased thickness of said top level of metallurgy reduces sensitivity to resistivity shifts associated with said silicided surface.